WHAT IS CLAIMED IS:

1. For use with an operational circuit comprising at least one high-impedance node, a pull-down circuit capable of pulling said high-impedance node down to ground when a pull-down (PD) signal driving said pull-down circuit is Logic 1, said pull-down circuit comprising:

a first pull-down N-channel transistor having a drain coupled to said high-impedance node, a gate coupled to said PD signal, and a source coupled to a common node;

a second pull-down N-channel transistor having a drain coupled to said common node, a gate coupled to said PD signal, and a source coupled to a ground rail;, wherein said first and second pull-down N-channel transistors are off when said PD signal is Logic 0 and are on when said PD signal is Logic 1; and

a gate-biasing circuit driven by said PD signal, wherein said gate-biasing circuit is off when said PD signal is Logic 1 and said gate-biasing circuit applies a Logic 1 bias voltage to said common node when said PD signal is Logic 0, said Logic 1 bias voltage creating a negative Vgs bias on said first pull-down N-channel transistor when said PD signal is Logic 0.

2. The pull-down circuit as set forth in Claim 1 wherein said gate-biasing circuit comprises a P-channel transistor having a gate coupled to said PD signal, a drain coupled to said common node, and a source coupled to a VDD power supply rail.

3. The pull-down circuit as set forth in Claim 2 wherein said operational circuit is a phase-locked loop (PLL).

4. The pull-down circuit as set forth in Claim 1 wherein said gate-biasing circuit comprises:

an inverter having an input coupled to said PD signal; and

a biasing N-channel transistor having a gate coupled to an output of said inverter, a source coupled to said common node, and a drain coupled to a VDD power supply rail.

5. The pull-down circuit as set forth in Claim 4 wherein said operational circuit is a phase-locked loop (PLL).

6. For use with an operational circuit comprising at least one high-impedance node, a pull-up circuit capable of pulling said high-impedance node up to a high voltage when a pull-up (PU*) signal driving said pull-up circuit is Logic 0, said pull-up circuit comprising:

a first pull-up P-channel transistor having a drain coupled to said high-impedance node, a gate coupled to said PU* signal, and a source coupled to a common node;

a second pull-up P-channel transistor having a drain coupled to said common node, a gate coupled to said PU* signal, and a source coupled to a VDD power supply rail, wherein said first and second pull-up P-channel transistors are off when said PU* signal is Logic 1 and are on when said PU* signal is Logic 0; and

a gate-biasing circuit driven by said PU* signal, wherein said gate-biasing circuit is off when said PU* signal is Logic 0 and said gate-biasing circuit applies a Logic 0 bias voltage to said common node when said PU* signal is Logic 1, said Logic 0 bias voltage creating a positive Vgs bias on said first pull-up P-channel transistor when said PU* signal is Logic 1.

7. The pull-up circuit as set forth in Claim 6 wherein said gate-biasing circuit comprises a biasing N-channel transistor having a gate coupled to said PU* signal, a drain coupled to said common node, and a source coupled to a ground power rail.

8. The pull-up circuit as set forth in Claim 7 wherein said operational circuit is a phase-locked loop (PLL).

9. The pull-up circuit as set forth in Claim 6 wherein said gate-biasing circuit comprises:

an inverter having an input coupled to said PU* signal; and

a biasing P-channel transistor having a gate coupled to an output of said inverter, a source coupled to said common node, and a drain coupled to a ground power rail.

10. The pull-up device as set forth in Claim 9 wherein said operational circuit is a phase-locked loop (PLL).